Simulation of Crosstalk between Several Interconnection Lines in CMOS Integrated Circuits

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Abstract - This work presents simulation of the crosstalk introduced by wiring in CMOS integrated circuits. Interconnections are modelled as lines with distributed parameters. Simulation results are shown on practical example. An electromagnetic simulator was used for calculation of coupled capacitances between conductors followed by the OrCad PSpice simulation to obtain the waveforms of output voltages on each line.

I. INTRODUCTION

Interconnection wiring is gaining a significant importance in speed of modern VLSI circuits. One of the reasons interconnections limit their performance are delay time and crosstalk effects [1]. One of the most challenging issues for semiconductor circuit design is how to overcome RC delays and crosstalk in the interconnect layers. Since the wiring may cover up to eighty percent of nowadays chip area, special care must be devoted to this problem. With larger dimensions and complexity of the chip, number of interconnections is increasing and also possibility of non-negligible crosstalk between them. Therefore, when designing for high speed circuits, designers have to pay special attention to the signal propagation through the wires.

Of course, a reliable and valuable simulation can help to the great extent to one’s insight into the circuit behavior [2]. A special case of two interconnection lines is considered in [3]. Results presented in this paper generalize these results and are applicable to any number of lines. We gave the method for computing maximal deviation of signal caused by crosstalk effect.

This paper is organized as follows: Section 2 deals with the capacitance model of interconnections. An electromagnetic simulator is used for calculation of the coupled capacitances between conductors. Section 3 describes an electrical model used in the circuit simulator. Presented results show that, as it has been expected, dominant crosstalk is between the neighbor conductors.

II. MODEL OF INTERCONNECTION LINES FOR DELAY TIME AND CROSSTALK SIMULATION

Thin film technology which is commonly used in modern CMOS circuits requires dealing with interconnection lines with distributed parameters. These lines are commonly treated as RC lines [1,2,4]. On higher frequencies the inductance of interconnections is not negligible and must be included in the model. Also in the case of more than two coupled interconnections, there exists capacitance between each pair of interconnections, i.e. there are \(N\cdot(N-1)/2\) coupled capacitances. As we will see, this number can be drastically reduced because many of these capacitances can be neglected. Figure 1 describes capacitance model of interconnection lines.

![Capacitance model of interconnections](image)

Fig. 1. Capacitance model of interconnections

For the cases \(N = 2\) and \(N = 3\) there are accurate analytic formulas for distributed capacitances \(c_{ij}\) between conductors [5]. For higher values of \(N\) there are no such formulas, so we have to use an electromagnetic simulator to calculate distributed capacitances. Simulator we used, Maxwell Student Version [6], is able to compute required capacitances directly from the model. In our approach, we used the same dimensions of conductors as used in [1]: \(W = 1.5 \, \mu\text{m}, \, T = 0.35 \, \mu\text{m}, \, S = 2.5 \, \mu\text{m}, \, H = 1 \, \mu\text{m}\). We obtained results for different values of \(N\) (5, 7, 9, 11 and 15).

Calculated coupled capacitances \(c_{ij}\) for the case \(N = 7\) are presented in Table I. All values are in pF/m.

It can be noticed that values of \(c_{ij}\) for \(N \geq 7\) almost do not depend on \(N\). Also, for \(|i - j| > 2\) capacitance \(c_{ij}\) is less than 1% of \(c_{ij}\), so they can be neglected. It means that every conductor influences two neighbor conductors on each side (for example, 4th conductor influences on 2nd, 3rd, 5th and 6th). So, we just need to consider three classes of...
capacitances: \( c_{ij}, c_{i,i+1}, \) and \( c_{i,i+2} \). In the first class, for the sake of symmetry there should hold:

\[
c_{1,3} \approx c_{4,4} \approx \ldots \approx c_{N-2,N-2}
\]

but \( c_{2,2} = c_{N-1,N-1} \) and \( c_{3,3} = c_{N,N-1} \) should be slightly different due to the boundary effects. Our calculation shows that maximum relative difference between capacitances \( c_{ij} \) for \( i = 3, 4, \ldots, N-2 \) is less than 1%, \( c_{2,2} = c_{N-1,N-1} \) is 5% greater and \( c_{3,3} = c_{N,N} \) is about 16% greater. So for the description of first class capacitances, we require three values.

**TABLE I**
CALCULATED CAPACITANCES FOR \( N = 7 \) CONDUCTORS

<table>
<thead>
<tr>
<th>( C_{ij} ) [pF/m]</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
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<td>1</td>
<td>130</td>
<td>14.5</td>
<td>2.33</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>14.5</td>
<td>117</td>
<td>14.1</td>
<td>2.29</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>2.33</td>
<td>14.1</td>
<td>116</td>
<td>13.9</td>
<td>2.29</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>2.29</td>
<td>13.9</td>
<td>114</td>
<td>13.9</td>
<td>2.29</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>2.29</td>
<td>13.9</td>
<td>116</td>
<td>14.1</td>
<td>2.33</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2.29</td>
<td>14.1</td>
<td>117</td>
<td>14.5</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2.33</td>
<td>14.5</td>
<td>130</td>
</tr>
</tbody>
</table>

Situation is similar in the second and third class. There holds

\[
c_{2,3} \approx c_{3,4} \approx \ldots \approx c_{N-2,N-1}
\]

and \( c_{i,i+1} \) is about 3% greater. In the third class, it is sufficient to consider just one value of capacitance and as we will see later, this class can be also neglected.

Finally for the circuit simulation we require just six values of capacitances. Calculated values in our example are:

\[
c_{11} = 1.325 \times 10^{-10} \text{ F/m}, \quad c_{22} = 1.20 \times 10^{-10} \text{ F/m}, \quad c_{33} = 1.14 \times 10^{-10} \text{ F/m},
\]

\[
c_{41} = 1.43 \times 10^{-11} \text{ F/m}, \quad c_{i,i+1} = 1.39 \times 10^{-11} \text{ F/m}, \quad c_{i,i+2} = 2.29 \times 10^{-12} \text{ F/m}
\]

**III. CROSSTALK SIMULATION IN TIME DOMAIN**

To simulate crosstalk, we used OrCad PSpice simulator. System of interconnection lines is modeled as cascade connection of multiport sections. An electrical circuit representing one section is shown on Figure 2.

Complete model of interconnections is formed by cascade connection of \( k = 15 \) sections. Total length of all interconnections in our example is \( l = 1300 \mu \text{m} \). Capacitances \( C_{ij} \) are calculated using the formula

\[
C_{ij} = \frac{c_{ij} \cdot l}{k}
\]

Inductive and resistive parameters ( \( L = L_{ij} \) and \( R = R_{ij} \) ) were calculated using formulas from [2]. Obtained values are: \( L = 157.79 \mu \text{H} \) and \( R = 5.2 \Omega \).

We considered \( N = 7 \) lines made of aluminum placed on the same distance \( d = 2.5 \mu \text{m} \). Equivalent circuit is shown in Figure 3.

All resistances are equal to \( R_p = 1 \text{k\Omega} \) and all input DC sources have the same voltage \( V_i = 5 \text{ V} \). Signal on the input of 4th line has periodical trapezoidal waveform with the frequency of 25 MHz and rise and fall times equal to 0.01 ns. Waveforms of output signals on lines 4, 5 and 6 are presented on Figures 4, 5 and 6, respectively.

As can be seen from the simulation results, the crosstalk effect can be noted at switching moments. Small graphs on each figure show the waveform of the impulse around switching moments (from 39 ns to 41 ns). Maximal deviation of signal at lines 5 and 6 due to the crosstalk are 700 mV and 110 mV respectively. Note that the ratio of these two values is almost the same as the ratio of the coupled capacitances between 4th and 5th line (\( c_{45} \)) and between 4th and 6th line (\( c_{46} \)). If we apply pulse signal to
the first line, similar values of maximal deviation are obtained (750 mV and 120 mV).

Now we will try to obtain maximal possible deviation due to the crosstalk. Let us modify the circuit, such that input signal on 2\textsuperscript{nd}, 3\textsuperscript{rd}, 5\textsuperscript{th} and 6\textsuperscript{th} line is pulse, and on 4\textsuperscript{th} line is constant (5 V, as in the previous case). Waveform of the output signal on line 4 is shown on Figure 7. Maximal deviation of the signal is now 1.9 V.

This value represents the maximum deviation of signal due to the crosstalk effect and should be compared with the noise margins of logical elements in order to verify proper design.

### III. CONCLUSION

In this work we considered crosstalk between several interconnections in modern CMOS VLSI circuits. The interconnections are represented as lines with distributed parameters over the entire length. First we used Maxwell SV electromagnetic simulator to compute coupled capacitances, then we presented an electrical model of interconnections and finally we used OrCad PSpice simulator to obtain output waveforms on each line. We calculated the deviations of the signal for different combination of the input voltages. Maximal signal deviation due to the crosstalk can be up to 41\% and it determines lower bound for the noise margins of the logical elements. Crosstalk effects can be reduced by increasing the distance between conductors ($d$).

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### REFERENCES


